

THIS MONTH WE CONTINUE our PC-based test-equipment series by building the T1004 digital logic IC tester and identifier. It is capable of testing 7400, 5400, and 4000 series IC's. In fact, the T1004 should be able to test any digital IC family that has the standard V_{CC} (+5V) and ground configuration (V_{CC} on the upper left corner of the IC package and ground on the lower right). On a 14-pin DIP that would mean that V_{CC} would be pin 14 and ground would be pin 7. The T1004 will accept 14-, 16-, 18-, 20-, 22-, and 24-pin DIP's.

The T1004 performs the following tests: Truth table, positive-going input threshold, negative-going input threshold, input hysteresis, output source capability under load, and an open-collector test. Additionally, the T1004 predicts (based on a best-guess analysis) what type of IC you are testing (HC, HCT, TTL, etc.). From now on, you'll find grab bags of unknown IC's very appealing because the T1004 has a feature that can help you identify those unknown digital IC's. If the IC being tested matches any of the IC's already in the IC database, the T1004 will find and display the names of those IC's. Running a complete test on one or all of those names will, in many cases, provide you with a comprehensive picture of the IC under test. The T1004 also lets you add IC's to the database. As we expand our IC support library we will make updated files available on the RE-BBS (515-293-2283, 1200/2400, 8N1).

General operation

Figure 1 shows the T1004 block diagram. The chip-select section is driven by the Front End section which we discussed in detail in our June

PC-BASED TEST BENCH



The T1004 digital logic IC tester and identifier can handle 7400-, 5400-, and 4000-series IC's.

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1992 issue; it selects and de-selects every other section in the T1004. The reference-voltage section provides a 2.5-volt reference for the analog-to-digital converter (ADC) section and also for the digital-to-analog converter (DAC) section. The pull-up or pull-down section (PUPD) is capable of providing a 10-kilohm pull-up or a 200-ohm pull-down to any or all of the test-socket pins (except the V_{CC} pin).

The DAC section produces a voltage (in 20-millivolt steps between 0 and 5 volts) which is fed to the DAC multiplexer (MUX)

section. The DAC MUX can apply the DAC voltage to one of pins 1 through 23 of the zero insertion force (ZIF) test socket. The DAC multiplexer can also disconnect the DAC voltage from the test socket. The ADC multiplexer can select a single voltage from one of pins 1 through 24 of the test socket and feed that voltage to the input of the ADC section. The socket-ground section supplies ground to one of six test-socket pins (pins 7-12) to connect the ground pin of the IC under test to ground.

Tests performed

• Truth-table test

During this description we'll use a 7432 quad 2-input OR gate as an example device. Because the 7432 is a 14-pin device, the socket-ground section grounds pin 7 of the test socket. The DAC section is disconnected from the socket. The device is looked up in the database and an input/output (I/O) mask is stored as three variables (or three 8-bit bytes). The I/O mask differentiates inputs from outputs. During subsequent testing, the I/O mask protects outputs from being inadvertently grounded. Next, a line of the truth table is

read into the three variables from the data base. The portions of those three variables which correspond to inputs are sent to the IC under test via the PUPD section.

At this point the ADC multiplexer and ADC sections scan every test socket pin for the resultant voltage. Voltages found to be greater than 2.4 volts are converted to highs, and those less than 2.4 volts are converted to lows. The highs and lows are converted to three 8-bit bytes that are compared to the bytes that were read in from the truth table. If they match, the IC has

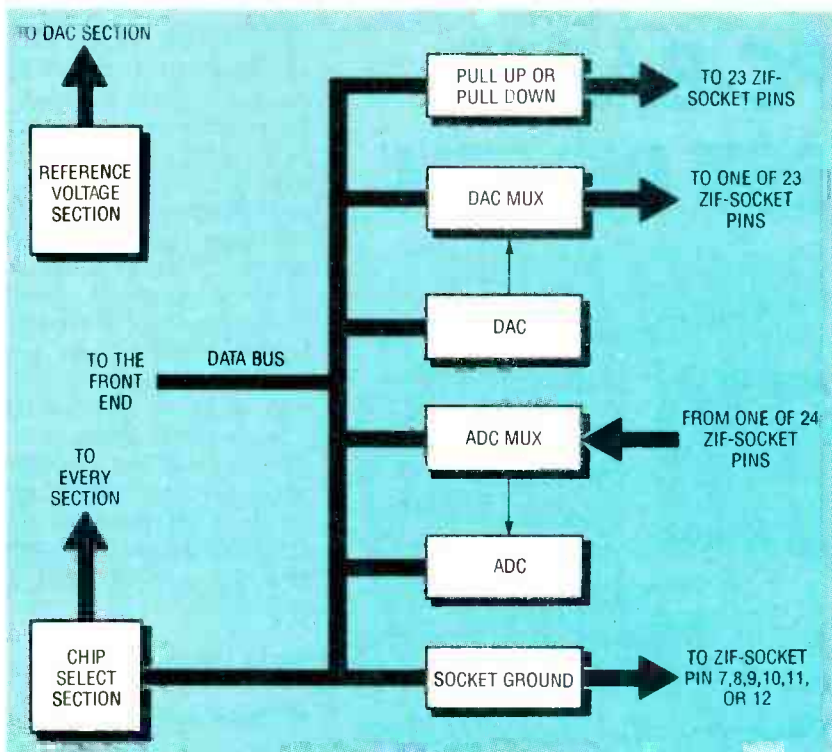


FIG. 1—T1004 BLOCK DIAGRAM. The Front End drives the chip-select section, which selects and deselects every other section in the T1004.

passed the first line of the truth table.

- **Low-to-high input test**

In this section three bytes are again sent to the test socket. The bytes are selected based on the following criteria: A known input pin on the IC under test is being held low. Additionally, when the pin being held low is taken high, a known output pin will change state. Working together, the DAC and DAC multiplexer sections take control of the input pin and slowly ramp its voltage from zero to the voltage level needed to cause the output pin to toggle. The voltage on the input pin is then read back and displayed on-screen next to the label "VT + :."

- **High-to-low input test**

In this section three bytes are again sent to the test socket. The bytes are selected based on the following criteria: A known input pin on the IC under test is being held high. Additionally, when the pin being held high is taken low, a known output pin will change state. The DAC and DAC multiplexer sections take control of the input pin and slowly ramp its voltage from +5 volts to the voltage level needed to cause the output pin to toggle.

The voltage on the input pin is then read back and displayed next to the label "VT - :."

- **Hysteresis**

Input hysteresis is the difference between the trigger point of an input being taken high and the trigger point of the same input when it is taken low. IC's such as a 7414 intentionally have a large amount of hysteresis to give them increased noise immunity. The T1004 calculates the hysteresis and displays it on the screen next to the label "HYS:." The T1004 calculates hysteresis as follows:

$$(VT+) - (VT-) = (\text{Hysteresis})$$

- **TTL input compatibility**

A TTL-compatible input must trigger when fed a voltage not larger than 2.4 volts. If VT+ is greater than 2.4 volts then the IC under test fails the test.

- **Output-load test**

The output-load test is performed by taking an output high and loading it with 200 ohms to ground for a very brief period. During the time that the load is present, the ADC reads the loaded voltage. This test will reveal weak or damaged gates, help to identify the gate type, and test for an open-collector condition.

Any of the tests described above may be omitted from the testing procedure. The testing process is defined by a *script*, which is a set of test instructions for a particular IC. Each IC has its own script which TSW or the end user writes to suit a particular IC. IC scripts are compiled using a program supplied by TSW.

Script tutorial

IC's not presently supported by the T1004 can be added to the existing database by the user. Each script contains the IC's name, whether the IC is an open-collector device, and its truth-table information. Scripts can be written using any ASCII text editor.

The easiest way to create a new script is to copy an existing script and edit it as needed. Once a script has been created, it can be compiled and added to the appropriate database. You can compile a script simply by selecting that option from the software menu. You will be asked to give the name of the script (example: S7400.TSW). The compiler will then open the script and get the IC name. Next, it checks to see if the target IC already exists in the database. If it already exists, then the previous version of the IC script will not be overwritten.

The delete function lets you remove any IC from the database. If the target IC does not exist in the database, then the compiler will compile the target script file and add the results to the database. The original script is written in a form that is easy for a person to follow. Once compiled, the script takes on a more compact form that can be used by the main testing program. Scripts for 14-pin IC's must be located in the directory "\TSW\ICTEST-D14\SCRIPTS." Similarly, scripts for 20-pin IC's must be located in the directory "\TSW\ICTEST-D20\SCRIPTS," and so on.

Take a look at Listing 1. The top line (TUTORIAL SCRIPT NUMBER 1) and the numbers down the left side (1-14) are not part of the script file. They have

been added for reference only, and should not appear in scripts that you write.

The symbols in the beginning of each line tell the software what kind of function is to be performed. A "?" tells the software that the two following variables are the IC's name and whether or not it is an open-collector device, respectively. A "#" tells the software that the letters "I," "O," "V," and "G" designate inputs, outputs, V_{CC} , and ground, respectively. "V" and "G" always represent V_{CC} and ground, respectively. The numbers "1" and "0" always represent a logic high and a logic low, respectively.

An "*" tells the software that following symbols designate the truth table of the IC under test, and that the data should be sent and the results should be read back. A "%" indicates that the following symbols designate the truth table of the IC under test, and that the data should be sent but not read back. A "/" tells the software that the following symbols designate the truth table used for the "low-to-high input threshold test" of the IC under test. A "I" says that the two following numeric variables designate the "low-to-high input threshold test" input and output pins, respectively. A "\\" indicates that the following symbols designate the truth table used for the "high-to-low input threshold test" of the IC under test. A "-" means that the following symbols designate the truth table used for the "output load test" of the IC under test. An "=" means that the following numeric variable designates the "output load test" output pin.

Let's take a closer look at the script in Listing 1. Line (1) must contain three string variables separated by commas. The first variable in the line must be a "?" which tells the software that the next character is the name of the IC. The IC name can contain nine characters. In this case the name is "7400." The next character on line (1) tells the software whether or not the IC being tested is an open-collector part; "Y" for open-collector parts

or "N" for parts without an open collector.

Line (2) represents the pin numbers of the IC being scripted. In this case the IC is a 14-pin package. Line (3) is the first line of the truth-table section. From that line the test software is able to determine whether to treat any given pin as an input or as an output. The line must be correct for the lines that follow to work correctly. If the IC being scripted has more than one input/output mode (a

LISTING 1 TUTORIAL SCRIPT NUMBER 1

```

-----
                                IC NAME
-----
(1) ?,7400,N

-----
                                PIN NUMBERS
-----
(2)  0 0 0 0 0 0 0 0 0 1 1 1 1 1
    1 2 3 4 5 6 7 8 9 0 1 2 3 4

-----
                                MAIN TRUTH TABLE
-----
(3) #,I,I,O,I,I,O,G,O,I,I,O,I,I,V
(4) *,0,0,1,0,0,1,G,1,0,0,1,0,0,V
(5) *,0,1,1,0,1,1,G,1,0,1,1,0,1,V
(6) *,1,0,1,1,0,1,G,1,1,0,1,1,0,V
(7) *,1,1,0,1,1,0,G,0,1,1,0,1,1,V

-----
                                LOW TO HIGH INPUT TEST
-----
(8) /,1,0,1,1,0,1,G,1,1,0,1,1,0,V
(9) |,2,3

-----
                                HIGH TO LOW INPUT TEST
-----
(10) \,1,1,0,1,1,0,G,0,1,1,0,1,1,V
(11) |,2,3

-----
                                OUTPUT LOAD TEST
-----
(12) -,0,0,1,0,0,1,G,1,0,0,1,0,0,V
(13) =,3

-----
(14) TSW ELECTRONICS
    14 PIN IC TEST SCRIPT
-----

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74245, for example), you should give a new "#" line just prior to the IC's mode change. You can use as many "#" lines as needed, and you can use them in any section of the script. In this case pin 1 is an input, pin 2 is an input, and pin 3 is an output. Pins 4–6 follow the same pattern and pin 7 is ground. Pin 8 is an output, pin 9 is an input, and pin 10 is an input. Pins 11–13 follow the same pattern and pin 14 is V_{CC} . If you check your data book you will see that this accurately describes the I/O of a 7400.

Line (4) begins with an "*"." That means that any "1's and "0's corresponding to inputs should be sent to the IC and that the "1's and "0's corresponding to outputs should be read back from the IC. If the "1's and "0's read back do not match the those predicted by the script then a fail condition exists. A 7400 is a quad 2-input NAND gate. The line tests all four gates at the same time. In line (4), pins 1, 2, 4, 5, 9, 10, 12, and 13 are all taken low. Each functioning NAND gate must respond by outputting a high. The results are read back and compared to the script. (Any error within the script will cause good IC's to fail the test). Lines (5) through (7) send and test the remaining truth-table conditions. An "*" can be used only in the truth-table section. Within that section, you can use as many "*" lines as you like.

Line (8) begins with a "/"." That character causes the "low-to-high input test" (LHT) to be performed. The LHT is used to determine the voltage that an input considers a high, or logic-1. The "1's and "0's corresponding to inputs are sent to the IC. Line (9) contains the character "I," which precedes the input and output pins to be used during the test. In this example pin 2 is used as the input and pin 3 is used as the output. When pin 2 is taken from low to high, pin 3 changes state. It is not important whether pin 3 goes from high to low or low to high, but only that a change of state occurs. The T1004 increases the voltage present at pin 2 (in 20-millivolt steps) until pin 3 changes states. The voltage on pin 2 is read back and displayed.

Lines (10) and (11) contain the character "\" and "I." They work in the same way except that the input voltage is swept from high to low. This test is used to determine VT-. Line (12) contains the character "-." That sends a truth table that must produce a high on one of the outputs. The next line contains the character "=", which tells the software which output pin is presently high. We could have chosen any

one of four outputs since they are all high. In this instance pin 3 is chosen, and loaded with 200 ohms to ground. The load test determines the sourcing capabilities of the gate, whether the part is open-collector or not, and provides clues that the software uses to predict the IC's family. The prediction of family or type should be considered a best guess (not absolute). Line (14) contains the text "TSW ELECTRONICS," which is there as an end-of-file marker for the compiler.

Listing 2 shows "TUTORIAL SCRIPT NUMBER 2." Line (1) indicates that the device is a 4040 and that it is not an open-collector device. Line (2) indicates that a 4040 is a 16-pin device. A 4040 is a 12-bit ripple counter. Line (3) indicates that pins 1-7 are outputs, pin 8 is ground, pin 9 is an output, pins 10 and 11 are inputs, pins 12-15 are outputs, and pin 16 is V_{CC} . Pin 10 is a falling-edge triggered clock input. Pin 11 is used to reset the counter, and is active only when high. Line (4) introduces the "%" command, which is similar to the "*" command, except that no test is performed; "%" should be used whenever you wish to send a byte to the IC without testing for a result.

In line (4) the RESET line (pin 11) and clock line (pin 10) are taken high. On that same line all of the outputs are shown low, which is an accurate representation of the effect that a reset would have on the outputs. Because line (4) is a "%" line, we do not actually test the outputs. On line (5) the reset line is released. On line (6) the clock is taken low activating the first output line (Q0). Because line (6) uses an "*" instead of a "%," the outputs will be tested for accuracy. The "%" command allows you to configure a device before you begin to test it. It can be used in any section and as often as you like. In the low-to-high input test, it is used to reconfigure the 4040 before we sweep the input. In this case, we are using the RESET input to determine the low-to-high threshold ($V_T +$).

The only pin that could be

used for the high-to-low input test is the CLOCK pin. Because clock input pins require fast transition times, they are not suitable for use in threshold tests. For that reason, the high-to-low input test is omitted for the 4040 IC. You can omit any section except the "?" section and the "TSW ELECTRONICS" section. A "#" must precede truth-table, threshold, or output-load tests. It must appear at least once or as often as needed.

LISTING 2 TUTORIAL SCRIPT NUMBER 2

```

-----
                        IC NAME
-----
(1) 7,4040,N

-----
                        PIN NUMBERS
-----
(2)  0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1
    1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6

-----
                        MAIN TRUTH TABLE
-----
(3) #,0,0,0,0,0,0,0,0,G,0,I,1,0,0,0,0,V
(4) %,0,0,0,0,0,0,0,0,G,0,1,1,0,0,0,0,V
(5) %,0,0,0,0,0,0,0,0,G,0,1,0,0,0,0,0,V
(6) %,0,0,0,0,0,0,0,0,G,1,0,0,0,0,0,0,V
(7) %,0,0,0,0,0,0,0,0,G,1,1,0,0,0,0,0,V
(8) %,0,0,0,0,0,0,0,1,G,0,0,0,0,0,0,0,V
(9) %,0,0,0,0,0,0,0,1,G,0,1,0,0,0,0,0,V
(10) %,0,0,0,0,0,0,0,1,G,1,0,0,0,0,0,0,V
(11) %,0,0,0,0,0,0,0,1,G,1,1,0,0,0,0,0,V
(12) %,0,0,0,0,0,0,1,0,G,0,0,0,0,0,0,0,V
(13) %,0,0,0,0,0,0,1,0,G,0,1,0,0,0,0,0,V
(14) %,0,0,0,0,0,0,1,0,G,1,0,0,0,0,0,0,V
(15) %,0,0,0,0,0,0,1,0,G,1,1,0,0,0,0,0,V
(16) %,0,0,0,0,0,0,1,1,G,0,0,0,0,0,0,0,V
(17) %,0,0,0,0,0,0,1,1,G,0,1,0,0,0,0,0,V
(18) %,0,0,0,0,0,0,1,1,G,1,0,0,0,0,0,0,V
(19) %,0,0,0,0,0,0,1,1,G,1,1,0,0,0,0,0,V

-----
                        LOW TO HIGH INPUT TEST
-----
(20) %,0,0,0,0,0,0,0,0,G,0,1,1,0,0,0,0,V
(21) %,0,0,0,0,0,0,0,0,G,0,1,0,0,0,0,0,V
(22) /,0,0,0,0,0,0,0,0,G,1,0,0,0,0,0,0,V
(23) |,1,1,9

-----
                        OUTPUT LOAD TEST
-----
(24) %,0,0,0,0,0,0,0,0,G,0,1,1,0,0,0,0,V
(25) %,0,0,0,0,0,0,0,0,G,0,1,0,0,0,0,0,V
(26) -,0,0,0,0,0,0,0,0,G,1,0,0,0,0,0,0,V
(27) =,9

-----
(28) TSW ELECTRONICS
    16 PIN IC TEST SCRIPT
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Detailed operation

We will use BASIC as an example language. As we've seen with previous peripherals, the first step in controlling the T1004 is to establish a base address and select the desired peripheral. The first bit of code will be: $BAS = 768 : OUT BAS + 31,4$ 768 (hex 300) is the factory-pre-set base address of the I1000. As noted earlier, this address is

DIP-switch selectable. Next, we have an "OUT TO BAS + 31." As you may recall, that address is reserved for peripheral selection. The T1004 has a unit, or peripheral address of "4." Consequently, if we send an "OUT TO BAS + 31" with a data byte of "4," the T1004 will be readied for full I/O operation.

The T1004 schematic has been split into two halves and shown in Figs. 2 and 3. Address lines A0-A4 (32 bytes) are used by the T1004 (or any other peripheral) to address its IC's, and A0 is the LSB of the address lines. (Lines A5-A9 are used by the I1000 only.) The chip-select section shown in Fig. 2 (IC23-IC25) contains two 74HCT138's (IC23 and IC24). Whenever their $\overline{G2A}$ and $\overline{G2B}$ lines are low and $G1$ is high, one of eight outputs will go low depending on the address present on the A, B, and C inputs. IC23 is active when BEN is high, \overline{SEND} is low, and RD is low. IC24 is active when BEN is high, \overline{SEND} is low, and WR is low. All but one of IC24's output lines drive the load line of the 74HCT573 latches. Because the load line of a 74HCT573 must see a high to store data, IC25 inverts the active lows produced by IC24.

The voltage-reference section, also in Fig. 2, is composed of IC26, R21, R1, IC9-a, and IC9-b. Trimmer R21 is adjusted for 2.5 volts at TP1. That provides the ADC section with a precise reference voltage. The reference voltage also passes through IC9-b and used by the DAC section.

An "OUT TO BAS + 7" will load a data byte into IC15 (a latch). DAC IC16, in combination with IC17-a, will produce between 0 and 5 volts which is proportional to the byte stored in IC15. The voltage produced will be a function of $n \times (5/255)$, where n is equal to the number loaded into the latch (IC15). A 500-ohm potentiometer (R22) is used to set the full-scale output voltage. If IC15 contains a value of 255, then R22 should be adjusted for 5 volts at IC17-a pin 1. The DAC multiplexer section is composed of IC18 through IC22. A latch (IC18) used to hold the DAC multiplexer address. The

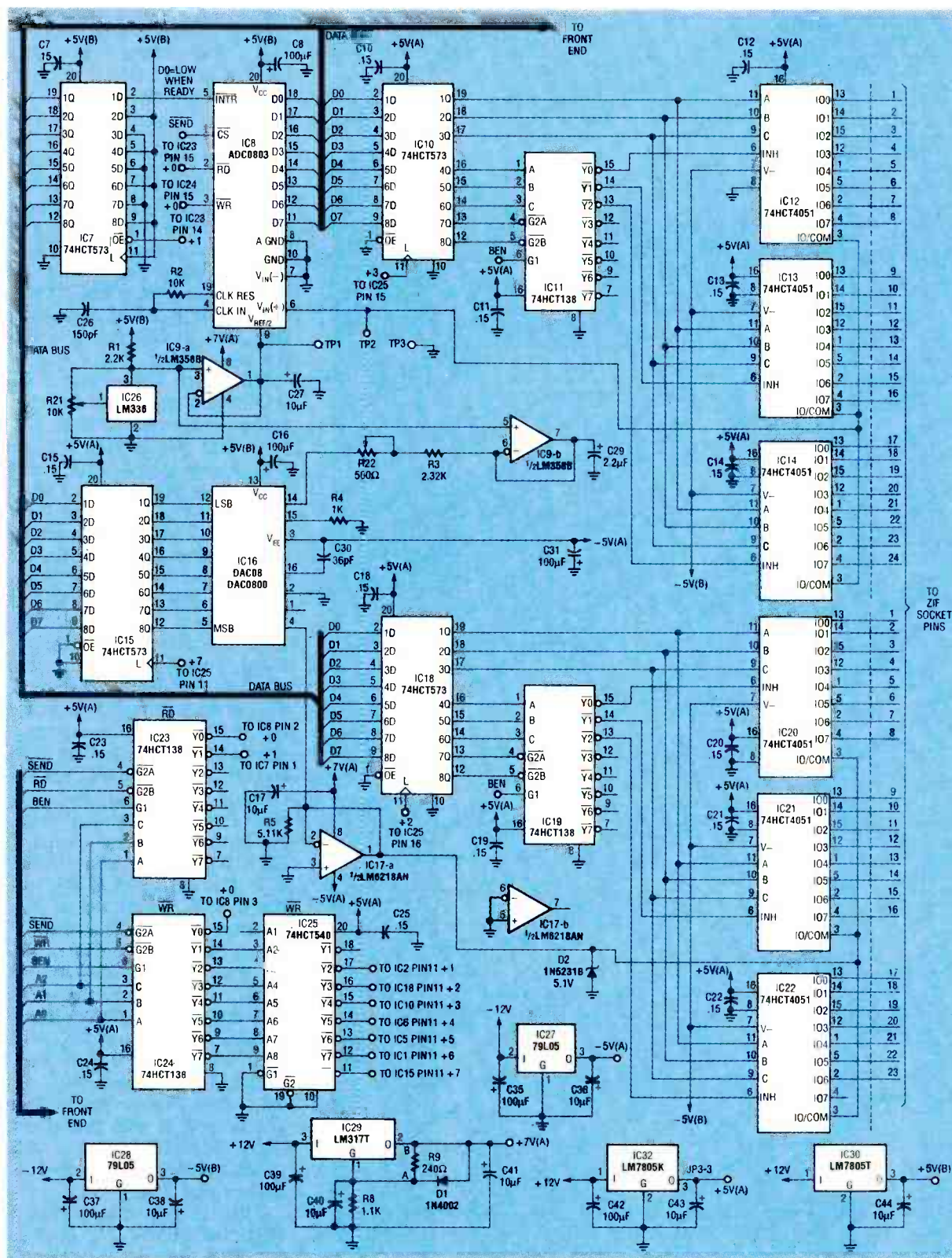


FIG. 2—IN THIS PORTION of the T1004 schematic, address lines A0–A4 are used to address IC's.

least significant three bits of the address are fed to each of three 8-bit multiplexers (74HCT4051). The remaining data lines are fed to IC19 (a

74HCT138), which activates only one of the multiplexer IC's (IC20–IC22). Assuming that the address byte sent to IC18 was less than 23, the DAC voltage is

then passed through to the test socket. If the address byte is 23 or greater, then the DAC voltage is disconnected from the test socket.

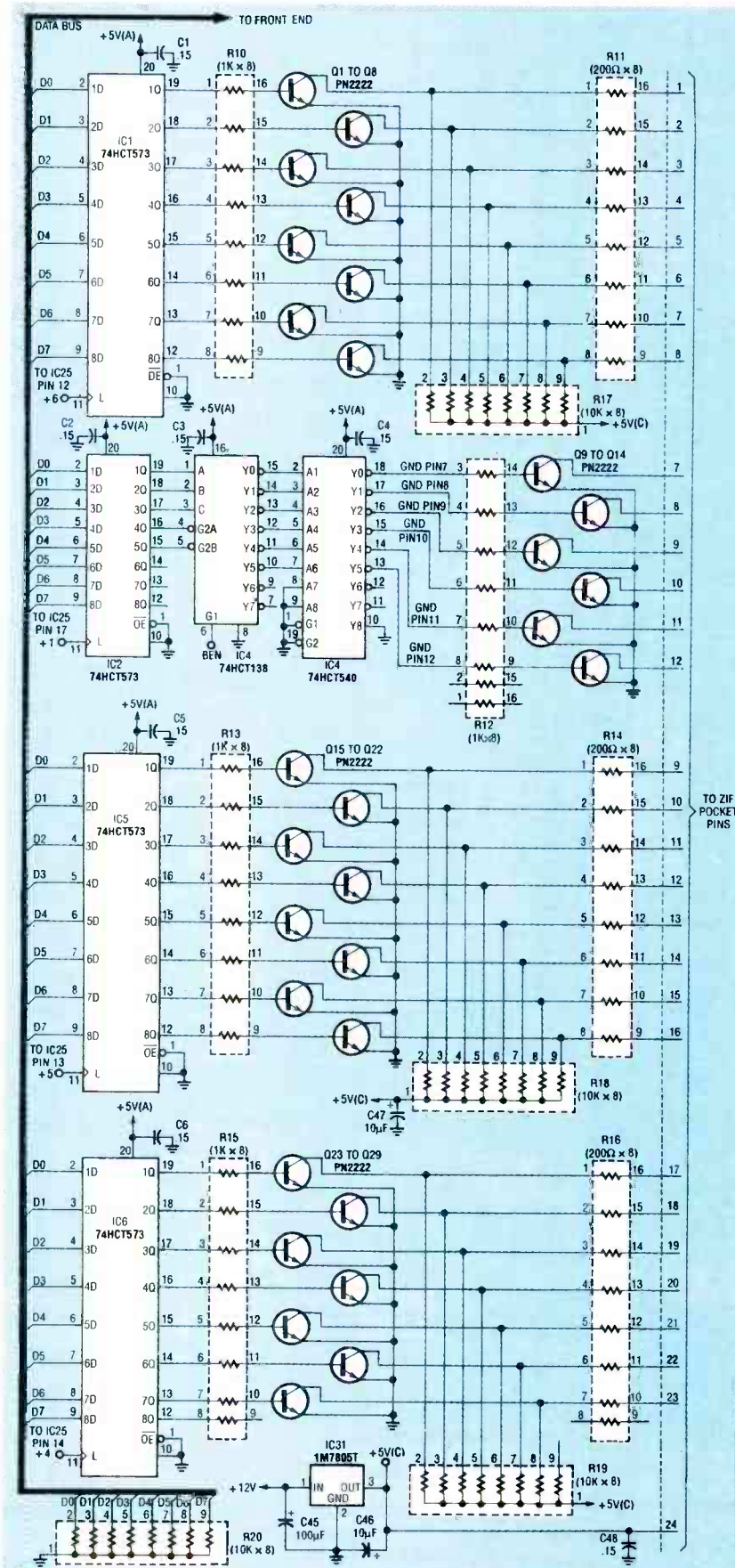


FIG. 3—THE PULL UP OR PULL DOWN section pulls any or all of the test socket pins high or low as needed.

Latch IC10 is used to hold the ADC multiplexer address. The least-significant three bits of the address are fed to each of three 8-bit multiplexers. The remaining data lines are fed to IC11, a 74HCT138, which activates only one of the multiplexer IC's (IC12-IC14). Assuming that the address byte sent to IC10 was less than 24, the ADC receives voltage from only one of the test socket pins. If the address byte is 24 or greater, then the ADC is disconnected from the test socket.

The pull up or pull down (PUPD) section, shown in Fig. 3, is composed of IC1, IC5, IC6, R10, R11, R13-R16, R17-R19, Q1-Q8, and Q15-Q29. This section pulls any or all of the test socket pins high or low as needed. The PUPD section is primarily responsible for truth-table functions. Three bytes are used to control the PUPD section. Byte-A controls test socket pins 1-8, Byte-B controls pins 9-16, and Byte-C controls pins 17-23. Pin 24 is reserved for V_{CC} only and is not affected by the PUPD or DAC sections. The sections controlled by Byte-A, Byte-B, and Byte-C are functionally identical, so we'll describe the Byte-A section only.

We'll assume that the number 85 (01010101) has been sent to IC1. The OUTPUT ENABLE line on IC1 (\overline{OE}) is grounded so the "Q" outputs must follow the "D" inputs. Pin 1 of DIP R10 will receive a high, pin 2 a low, pin 3 a high, and so on. Resultantly, the base of Q1 will be taken high connecting ground to R11 pin 1. That causes pin 1 of the test socket to be pulled low through 200 ohms. Because the base of Q2 is low, it will not conduct. That allows R17 pin 3 to pull R11 pin 2, and subsequently the test socket pin 2, high.

The IC ground section consists of IC2-IC4, R12, and Q9-Q14. Any byte latched into IC2 is passed directly to IC3. Byte values ranging from 0 to 5 transition to a low one of IC3's output lines. IC4 inverts the signals which are then fed through R12 to the bases of Q9-Q14. Only one line is active at a time, thus ensuring that

only one transistor is conducting at any given moment. Transistor Q9 is selected when driving a 14-pin device and Q14 would be used when driving a 24-pin device.

Regulator IC27 and its associated components produce -5 volts, which is used by the DAC (IC16). Regulator IC28 and its associated components produce -5 volts for the multiplexers (IC12-IC14 and IC20-IC22). Regulator IC29 and its associated components produce +7 volts, which the op-amps require in order to produce a full 5-volt output swing. Regulator IC31 and its associated components produce +5 volts for the IC being tested. Regulator IC30 and IC32 and their associated

components produce +5 volts for all the remaining IC's. Regulator IC31 produces +5 volts and is dedicated to supplying V_{CC} to the test socket and +5 volts to the pull-up resistors R17-R19.

Construction

To build the T1004 peripheral, a PC board is recommended. You can either buy a PC board from the source mentioned in the Parts List or make your own from the foil patterns we've provided. Note that the parts for the Front End are contained on the T1004 board shown with a dark line around them in the Parts-Placement diagram of Fig. 4. There is a separate Parts List for the Front

End, which was discussed in detail in the June issue. Do not confuse the two lists of parts, or where they go on the board. Also, for many of the capacitors, notice that there are three holes on the board, with two of them electrically the same. The holes accommodate capacitors with different lead spacing. Use whichever pair of holes on the printed-circuit board that best fits the capacitors you intend to use for the project.

One of the voltage regulators (IC32) is in a TO-3 case that must be mounted on the back panel of the T1004 case. Mount the regulator, along with an appropriate heatsink, on the back panel and hardwire it to the board. Figure 5 shows the com-

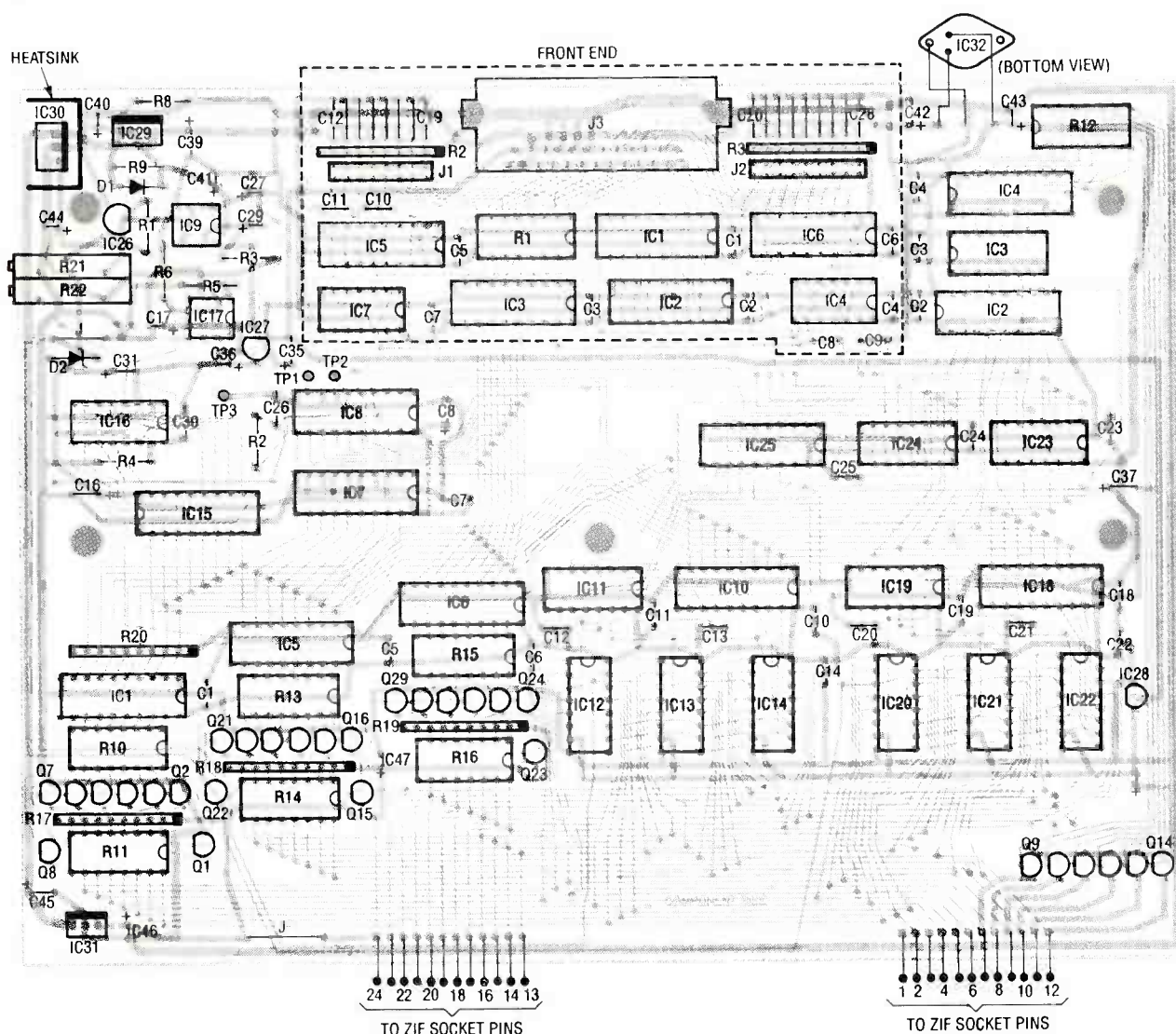
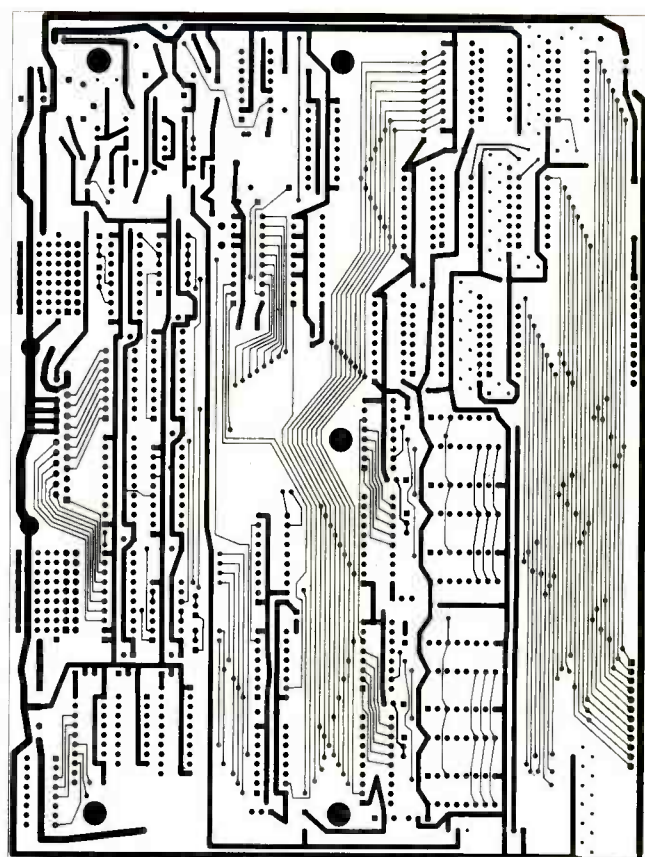
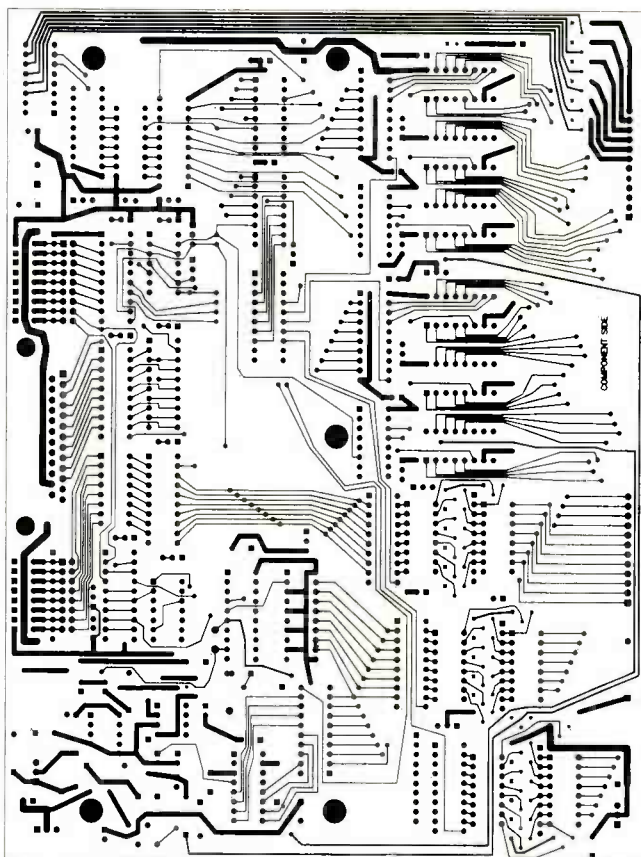


FIG. 4—PARTS-PLACEMENT DIAGRAM. The parts for the Front End are shown with a dark line around them. There is a separate Parts List for the Front End, so don't confuse the two lists of parts, or where they go on the board.



6 11/16 INCHES

T1004 COMPONENT SIDE.

6 11/16 INCHES

T1004 SOLDER SIDE.

T1004 PARTS LIST

All resistors are 1/4-watt, 5%, unless otherwise noted.

R1—2200 ohms
R2—10,000 ohms
R3—2320 ohms, 1%
R4—1000 ohms
R5—5110 ohms, 1%
R6—2050 ohms, 1%
R8—1100 ohms
R9—240 ohms
R10, R12, R13, R15—1000 ohms, 16-pin DIP

R11, R14, R16—200 ohms, 16-pin DIP
R17—R20—10,000 ohms, 10-pin SIP
R21—10,000 ohms, multiturn trimmer potentiometer
R22—500 ohms, multiturn trimmer potentiometer

Capacitors

C1—C7, C10—C14, C18—C25, C48—0.15 μ F, polystyrene
C8, C16, C31, C35, C37, C39, C42, C45—100 μ F, electrolytic
C9, C15, C28, C32, C33, C34—not used
C17, C27, C36, C38, C40, C41, C43, C44, C46, C47—10 μ F, electrolytic
C26—150 pF, mica

C29—2.2 μ F, electrolytic
C30—36 pF, mica

Semiconductors

IC1, IC2, IC5, IC6, IC7, IC10, IC15, IC18—74HCT573 octal latch
IC3, IC11, IC19, IC23, IC24—74HCT138 demultiplexer
IC4, IC25—74HCT540 octal buffer
IC8—ADC0803 8-bit A/D converter
IC9—LM358 dual op-amp
IC12—IC14, IC20—IC22—74HCT4051 8-bit multiplexer

IC16—DAC0800 or DAC08 D/A converter

IC17—LM6218AN op-amp
IC26—LM336 voltage reference
IC27, IC28—79L05 voltage regulator
IC29—LM317T voltage regulator
IC30, IC31—LM7805T voltage regulator
IC32—UA7805K voltage regulator (TO-3 case)

D1—1N4002 diode

D2 1N5231 5.1-volt Zener diode

Q1—Q29—PN2222 NPN transistor

Miscellaneous: 24-pin ZIF socket, TO-220 heatsink, TO-3 heatsink, PC board, instrument case, wire, solder, etc.

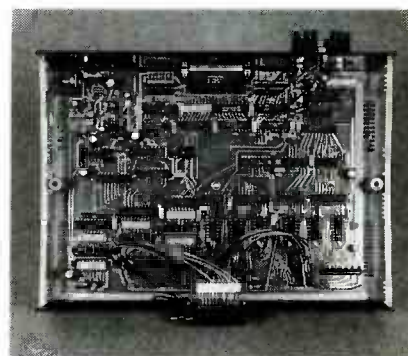


FIG. 5—THE COMPLETED T1004. One of the voltage regulators, IC32, must be mounted on the back panel of the T1004 case.

pleted T1004 board. When you use the T1004, position the IC's you want to test as shown in Fig. 6.

Software

Each peripheral has its own software program to control its operation. All of the programs

end up in one directory as you add more peripherals. Software for the I1000 and the entire series of peripherals, including the T1004, can be downloaded from the RE-BBS (516-293-2283, 1200/2400, 8N1) as a self-unarchiving zip file called T1004.EXE. Both compiled and uncompiled software is included. Software is included free with the purchase of any peripheral from the source that is mentioned in the Parts

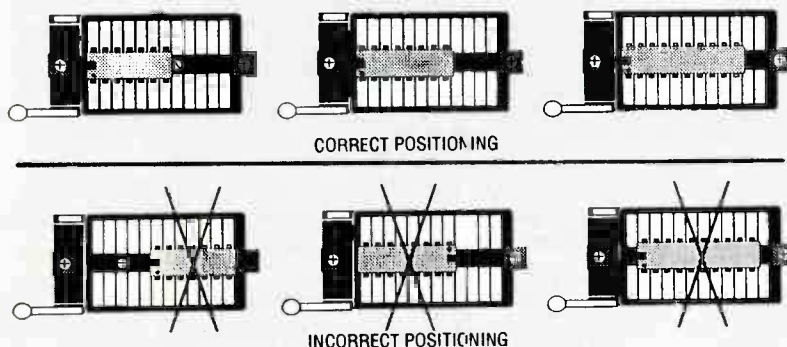
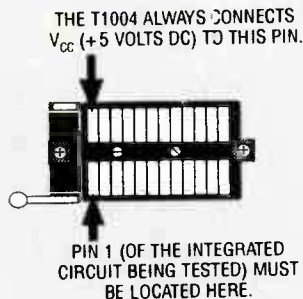


FIG. 6—BE SURE TO POSITION the IC's you want to test in the test socket as shown here.

FRONT-END PARTS LIST

Resistors

- R1—33 ohms, 16-pin DIP resistor
- R2—2200 ohms, 10-pin SIP resistor
- R3—1000 ohms, 10-pin SIP resistor

Capacitors

- C1—C7—0.15 μ F, 50 volts, monolithic or polystyrene
- C8—C11, C20—C28—1500 pF, 63 volts, polystyrene
- C12—C19—220 pF, 100 volts, ceramic disc

Semiconductors

- IC1—74LS573D octal latch
- IC2—74LS688D 8-bit magnitude comparator
- IC3—74LS245D octal transceiver
- IC4—74LS02D quad 2-input NOR gate
- IC5, IC6—octal buffer
- IC7—74LS08D quad 2-input AND gate

Other components

- J1—16-pin male header
- J2—18-pin male header
- J3—male PC-mount DB25 connector

Miscellaneous: 17 shorting blocks (for J1 and J2)

Note: The following items are available from TSW Electronics Corp., 2756 N. University Drive, Suite 168, Sunrise, FL 33322 (305) 748-3387:

- I1000 kit—\$65.00
- I1000 PC board only—\$35.00
- I1000, assembled and tested—\$77.00

- 6-foot interface cable (DB-25-6)—\$12.95

- T1001 kit (includes PC board, all listed parts, project case, and pre-assembled front and rear panels)—\$149.00

- T1001 PC board only—\$49.00

- T1001, assembled and tested—\$179.00

- T1001 software (included free with T1001 order)—\$10.00

- Capacitor kit (unmeasured)—\$21.00

- Capacitor kit (measured to within 1%)—\$26.00

- T1003 kit (includes PC board, all listed parts, project case, and pre-assembled front and rear panels)—\$159.00

- T1003 PC board only—\$59.00

- T1003, assembled and tested—\$189.00

- T1003 software (included free with T1003 order)—\$10.00

- T1004 kit (includes PC board, all listed parts, project case, and pre-assembled front and rear panels)—\$239.00

- T1004 PC board only—\$79.00

- T1004, assembled and tested—\$249.00

- T1004 software (included free with T1004 order)—\$10.00

Add \$5.00 S&H to any order. Check or money order only.

List. (Software can also be purchased from that same supplier if you're not buying anything else from them and you have no

way of downloading it from the RE-BBS.) With the T1004, you are on your way to automatic troubleshooting. R-E

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