

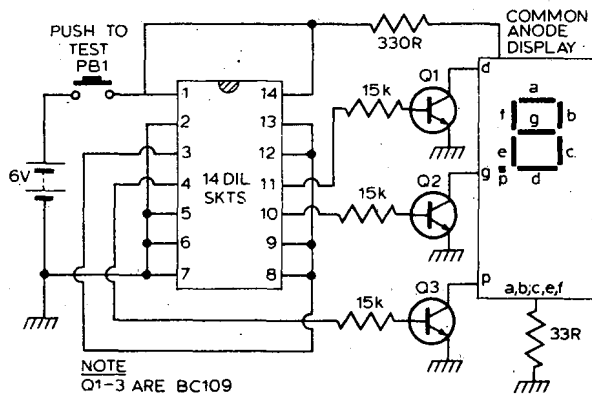
Frequency meter overflow indicator

After Gregory Freeman of Nairne had built the ETI 118 digital frequency meter, he found that the lack of an overflow indication was rather disconcerting. As a result, he built this little circuit, which latches the overflow output from the ETI 533 digital display module and resets it after a pre-determined period.

Although the circuit was originally intended for the ETI 118, it should be fairly easy to add it to any of the projects which use the 533 module.

Operation is fairly straightforward. When the overflow output of the 533 pulses high, it sets the latch formed by the 4011. This lights the LED via the transistor which will remain on until the 555 resets it.

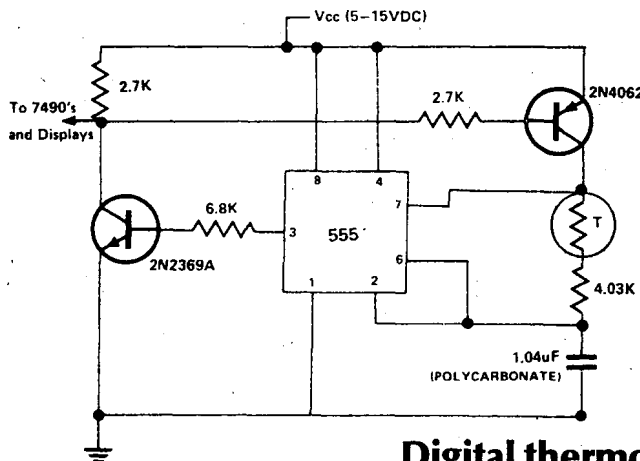
The 555 is operating in the monostable mode, being triggered about every three seconds by the timebase output of the DFM (which is pin G on the board).



CMOS gate identifier

The circuit can be used to distinguish four types of dual input gates — AND, OR, NAND, NOR — it is also a quick method of checking IC function. If

an AND gate is inserted into the socket, an A appears on the LED. An O denotes an OR gate. The decimal point is used to denote inverted function, i.e. A is an NAND gate.

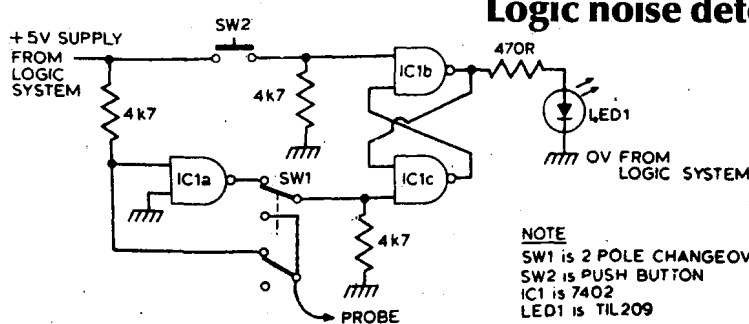


Digital thermometer

This circuit we haven't tried yet but it looks very good, anybody who tries it, let us know how you get on. The circuit's output frequency varies in a nearly linear manner from 38 to 114Hz as the temperature changes from 37°F to 115°F. The 555 is set up in the normal astable configuration with one resistor replaced by a thermistor/resistor network and other replaced by a transistor. The transistor's near zero on-resistance and very high off-resistance

results in equal charge and discharge intervals that depend only on the thermistor/resistor network. The thermistor is one with a value of 5000 ohms at 25°C and a resistance ratio of 9.06:1 over the temperature range 0°C to 50°C. The capacitors need to be temperature stable and may need to be hand selected and added to give the best results. It would seem that a similar circuit for Centigrade might also be possible — any ideas?

Ever since the advent of binary logic, spurious noise spikes and pulses have been the curse of the designers of even elementary systems. This circuit will help detect 'noisy' logic levels. With SW1 in position 1, any logic zero spikes occurring on a steady logic '1' will set the R-S latch and the LED will be illuminated. With SW1 in position 2, an extra inverter is brought in, and the circuit will be triggered by any logic '1' spikes.



Logic noise detector

NOTE
SW1 IS 2 POLE CHANGEOVER
SW2 IS PUSH BUTTON
IC1 IS 7402
LED1 IS TIL209